

METHOD FOR TESTING MEMORIES
WITH SEAMLESS DATA INPUT/OUTPUT
BY INTERLEAVING SEAMLESS BANK COMMANDS

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a method for testing memories, and more particularly to a method for testing memories with seamless data input/output by interleaving seamless bank commands so as to detect a weakened memory.

2. Description of Related Art

While dynamic random access memories (DRAM) are manufactured by 0.2 μm process technology or an advanced manufacturing process, a power supply is lower than 3.3 volts, and a clock rate applied is higher than 133 megahertz, and the DRAM performance is then more and more sensitive to noise from external command signals, address signals, input data signals, and intrinsic noise raised from internal circuitry. For such consideration, DRAM designers have to carefully design memory circuits to provide correct data storage/access paths from each memory cell. On the other hand, DRAM manufacturing engineers must carefully control process conditions to guarantee target device/circuit performance. Even so, weakened memory cells still sometimes exist in DRAM chips and weakened data are probably stored. Thus, a challenge to test engineers is to provide a testing program to screen those memories and assist circuit designers to find critical data access paths and to cover device weakness.

1 A memory testing program is assembled by a pin condition setting, and
2 a data access pattern. The pin condition setting includes setting of
3 commanding pins, addressing pins and I/O pins. The data access pattern is
4 used to define word-by-word data access paths and its corresponding
5 operational clock rate. The pin condition setting, which includes true table
6 setting and logic high/low voltage setting, is based on DRAM specification
7 reference to data sheet. The data access pattern is, on the other hand, created
8 by specific testing purposes. For instance, a one-dimensional row access
9 pattern for accessing memory cells on a fixed word line (W/L) is applied to
10 check word line continuity; and a one-dimensional column access pattern
11 for accessing memory cells located on the same column is applied to check
12 bit line (B/L) continuity. In the book "Testing Semiconductor Memory"
13 written by A.J. van de Goor, published by John Wiley & Sons, there are
14 traditional two-dimensional checkboards, GALPAT, sliding diagonals,
15 butterfly patterns etc. for providing better fault coverage.

16 Usually, programming commands loops are used to carry out the access
17 patterns mentioned above. For example, a memory has four banks (#0-#3)
18 are shown in Figs. 5, 6A and 6B, a programmable cycling control command
19 "Bank active - Write or Read - Bank pre-charge" is applied in the single
20 bank (Bank #0), wherein the burst length in Figs. 5, 6A and 6B is 4. In Fig. 5,
21 while a "write" command is generated, data having four clock lengths are
22 outputted from data input/output terminals (DQ). In Figs. 6A and 6B, while
23 a "read" command is generated, data in DQ respectively has two and three
24 clock latency. This kind of cycling command is generally used to check

1 basic functions of DRAM chips, however data in DQ are not
2 inputted/outputted seamlessly.

3 With reference to Figs. 7, 8A and 8B, those figures are similar to Figs. 5,
4 6A and 6B, with a difference being that a programmable cycling command
5 "Bank active - Write with auto pre-charge or Read with auto pre-charge" is
6 applied in a single bank (Bank #0). This kind of loop is used to check
7 functions of an auto pre-charge.

8 With reference to Figs. 9 to 12, those figures disclose an interleave bank
9 operation. Two banks interleave and four banks interleave operations are
10 shown in Figs. 9~10 and Figs. 11~12 respectively. Such repeated operations
11 are capable to do seamless input/output (I/O) checks for examining I/O
12 performance. Clearly, the operations shown in Figs. 9 to 12 suffer larger
13 noise due to more compact I/O operations than those shown in Figs. 5 to 8.
14 Although DQ in Figs. 9 to 12 are inputted/outputted data seamlessly, control
15 pins of memory still do not receive seamless controlling commands. Even
16 four banks (Bank #0, #1, #2 and #3) receive initial "active" commands, the
17 control pins still retain in a "wait" situation at 14th, 15th, 18th, 19th, 22nd,
18 23rd, 26th, 27th, clock cycles. Thus the commands shown in Figs. 9 to 12 are
19 not sufficient to detect weakened memory cells.

20 To overcome these shortcomings, the present invention tends to
21 provide a method for testing a memory with seamless data input/output by
22 interleaving seamless bank commands to mitigate and obviate the
23 aforementioned problems.

24 SUMMARY OF THE INVENTION

1 The main object of the present invention is to provide a method for
2 testing memories with seamless data input/output by interleaving seamless
3 bank commands so as to provide seamless data and commands to data
4 input/output pins and control pins of the memory.

5 The second object of the present invention is not only to provide a
6 method that suits testing SDRAMs, but also suits testing DDR DRAMs and
7 RDRAMs.

8 To achieve the main object, the method in accordance with the present
9 invention comprising steps of :

10 transferring data to data input/output (I/O) pins of memories
11 seamlessly;

12 inputting control commands to control pins of the memories
13 seamlessly.

14 Thus control pins and data input/output pins of memories receive heavy
15 loading due to the seamless control commands, whereby the weakened
16 memories are easily to detect.

17 Other objects, advantages, and novel features of the invention will
18 become more apparent from the following detailed description when taken
19 in conjunction with the attached drawings.

20 BRIEF DESCRIPTION OF THE DRAWINGS

21 Figs. 1A to 1C respectively show a memory testing timing sequence
22 view of first to third embodiments in accordance with the present invention;

23 Figs. 2A to 2D respectively show a memory testing timing sequence
24 view of fourth to seventh embodiments in accordance with the present

1 invention;

2 Figs. 3A to 3C respectively show a DDR-DRAM memory testing
3 timing sequence view in accordance with the present invention;

4 Figs. 4A and 4B respectively show a RDRAM memory testing timing
5 sequence view in accordance with the present invention;

6 Fig. 5 is a timing sequence view of a conventional memory testing
7 method showing data writing in a single bank;

8 Figs. 6A and 6B are timing sequence views of a conventional memory
9 testing method showing data reading in a single bank;

10 Fig. 7 is a timing sequence view of a conventional memory testing
11 method showing data writing and auto pre-charge in a single bank;

12 Figs. 8A and 8B are timing sequence views of a conventional memory
13 testing method showing data reading and auto pre-charge in a single bank;
14 and

15 Figs. 9, 10A, 10B, 11, 12A and 12B are timing sequence views of a
16 conventional memory testing method showing data reading/writing in
17 multi-banks °

18 DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

19 The present invention is a method for testing a memory by providing
20 seamless control commands and data, wherein the memory has at least two
21 banks. By providing seamless control commands and data, the control pins
22 and data input/output pins of the memory receive heavy loading due to the
23 seamless control commands. For SDRAMs and DDR-DRAMs, control
24 commands and data are seamlessly inputted/outputted at each clock cycle.

1 For RDRAMs, control commands are inputted at each "command packet",
2 whereby data are inputted/outputted at each "data packet" and memories are
3 in heavy loading status. By providing heavy loading to memories, it is easy
4 to detect weakened memories.

5 In the following description, "DQ" that appears in figures in
6 accordance with the present invention is used to represent data input/output
7 terminals.

8 With reference to Figs. 1A, 1B and 1C, timing sequence views
9 respectively having burst lengths of 2, 4 and 8 with different cycling control
10 commands are shown.

11 With reference to Fig. 1A, after banks #0 ~ #3 serially receive "active"
12 commands with two clock cycle intervals, control commands "write with
13 auto pre-charge" are inputted to each bank at appropriate intervals. Thus
14 after the bank #3 receives the initial "active" command, control commands
15 (including "active" and "write with auto-pre charge") are sequentially
16 inputted to the banks #0~#3 at each clock cycle, whereby data input/output
17 terminals (DQ) have seamless data input/output and remains in a heavy
18 loading status.

19 With reference to Fig. 1B, the burst length is 4 and the cycling control
20 commands are programmed as "active, write, write, bank pre-charge", and
21 the data input/output terminals (DQ) still have seamless data input/output.

22 With reference to Fig. 1C, the burst length is 8. Different types of
23 cycling control commands are provided to each bank. In the bank #0, the
24 control commands are "active, write, write, bank pre-charge, active, bank

1 pre-charge, active, bank precharge". In the bank #1, the control commands
2 are "active, bank pre-charge, active, write, write, bank pre-charge, active".
3 In the bank #2, the control commands are "active, bank pre-charge, active,
4 bank pre-charge, active, write, write". In the bank #3, the control commands
5 is another type that differs from the control commands in banks #0 ~ #2.
6 Although the control commands types for each bank are different, control
7 pins and data input/output terminal (DQ) still remain in a heavy loading
8 status.

9 With reference to Figs. 2A and 2B, cycling control commands "active,
10 bank with auto pre-charge" are applied to each bank with different
11 latencies(2 and 3). At each clock cycle, one of the banks (bank #0 ~ #3) still
12 receives a control command, and the data input/output terminals (DQ) has
13 seamless data input/output.

14 The present invention not only provides seamless data and control
15 commands to data input/output terminals (DQ) and control pins, but also
16 depends on memory testing requirement to provide a purposeful interrupt or
17 delay to control commands.

18 With reference to Fig. 2C, a control command "CKE" is inserted in the
19 cycling control commands, thus the next control command has a one clock
20 cycle delay, whereby the operating accuracy of memories is easily detected.

21 With reference to Fig. 2D, a mask control command "DQM" is inserted
22 in the cycling control commands at a purposeful clock cycle, thus data at the
23 purposeful clock cycle are masked.

24 The present invention also suits application for DDR-DRAMs and

1 RDRAMs.

2 With reference to Figs. 3A, 3B and 3D, timing sequence views of
3 testing DDR-DRAMs with data writing/reading are respectively shown.
4 The cycling control commands of DDR-DRAMs are similar to the control
5 commands mentioned above. The difference between the data
6 inputting/outputting status of Figs. 3A, B and D, and the data
7 inputting/outputting status mentioned above is that two data appear at the
8 same clock cycle.

9 With reference to Figs. 4A, 4B and 4C, timing sequence views of
10 testing RDRAMs with data writing/reading are respectively shown, wherein
11 control commands and data are inputted/outputted seamlessly at each
12 "packet" not "clock cycle".

13 Although the present invention has been explained in relation to its
14 preferred embodiment, it is to be understood that many other possible
15 modifications and variations can be made without departing from the spirit
16 and scope of the invention as hereinafter claimed.